# Amiga

# A500_R6

Rev.1.37 (02.09.2012)

# Revision History

| REV | DESCRIPTION | DATE | APRVL | MANAGER |
|---|---|---|---|---|
| - | For older Revision 3/5 boards | | | |
| | see schematic 312511-01 | | | |
| 1 | PCB Revision 6a/7 Production | 04/27/89 | GRR | |

# Jumpers and Stuff

| REF | TYPE | DESCRIPTION | PAGE |
|---|---|---|---|
| JP1 | BLOB | Keyboard Reset | 7 |
| JP2 | BLOB | Memory Addr. C0 vs 08 | 2 |
| JP3 | BLOB | Expansion RAS Select | 3 |
| JP4 | BLOB | NTSC/PAL Selection | 2 |
| JP5 | BLOB | Genlock Clock Select | 2 |
| JP6 | BLOB | 7MHz Clock Option | 7 |
| JP7 | BLOB | Expansion/Tick Option | 3/6 |
| JP8 | BLOB | Light Pen Port Select | 6 |
| JP10 | BLOB | RS232 Audio I/O Cutout | 4 |
| JP11 | BLOB | TTL vs RS170 Comp Sync | 5 |

# Connectors

| REF | TYPE | DESCRIPTION | PAGE |
|---|---|---|---|
| CN1 | DB9P | Mouse/Joystick 1 | 2 |
| CN2 | DB9P | Mouse/Joystick 2 | 2 |
| CN3 | RCA-J | Right Audio Output | 4 |
| CN4 | RCA-J | Left Audio Output | 4 |
| CN5 | DB23S | External Floppy | 7 |
| CN6 | DB25P | RS232 Serial Port | 6 |
| CN7 | DB25S | Parallel Printer Port | 6 |
| CN8 | SQ DIN | Power Supply Connector | 8 |
| CN9 | DB23P | Video Output | 5 |
| CN10 | RCA-J | Composite Video | 5 |
| CN11 | DIL-34 | Internal Floppy Signal | 7 |
| CN12 | SIL-4 | Internal Floppy Power | 8 |
| CN13 | SIL-8 | Keyboard Connector | 6 |
| P1 | EDGE86 | Expansion Connector | 7 |
| CNX | RA-56H | Mem. Exp. Main-Board | 3 |

# ECO Log

| ECO NUMBER | DESCRIPTION | DATE |
|---|---|---|
| 880283 | Add E Clock Termination | 03/03/89 |

# Signal Glossary

| SIGNAL | DESCRIPTION (AREA) | PAGES |
|---|---|---|
| 28MHZ | 28.63636 MHz Master Clock | 2 |
| 7MHZ | 7.15909 MHz Processor Clock | 2,5 |
| A[23:1] | Processor Address Bus (68000) | 2,3,7 |
| ACK | Data Acknowledge (Parallel Port) | 6 |
| AS | Address Strobe (68000) | 2,7 |
| AUDIN | Audio Input (RS232 Port) | 4,6 |
| AUDOUT | Audio Output (RS232 Jack) | 4,6 |
| BEER | Bus Error (68000) | 2,7 |
| BG | Bus Grant (68000) | 2,7 |
| BGACK | Bus Grant Acknowledge (68000) | 2,7 |
| BLISS | Blitter Slowdown (Chips) | 2 |
| BLIT | Chip Memory Access (Chips) | 2,7 |
| BR | Bus Request (68000) | 2,7 |
| BUSY | Device Busy (Parallel Port) | 6 |
| CASL/U | Column Address Strobe (DRAM) | 2,3 |
| CCK/CCKQ | Color Clock / Quadrature (Chips) | 2,4,7 |
| CDAC | 7.15909 MHz Quadrature Clock (Chips) | 2,5,7 |
| CHNG | Media Change (Floppy) | 6,7 |
| CLKRD/WR | Read-Time Clock Read / Write (RTC) | 2,9 |
| COMP | Monochrome Composite Video (Video) | 5 |
| CSYNC | Composite Sync (Video) | 2,5 |
| CTS | Clear to Send (RS232 Port) | 6 |
| D[15:0] | Processor Data Bus (68000) | 2,3,6,7 |
| DIR | Step Direction (Floppy) | 6,7 |
| DKRD | Disk Read Data (Floppy) | 4,7 |
| DKWD | Disk Write Data (Floppy) | 4,7 |
| DKWE | Disk Write Enable (Floppy) | 4,7 |
| DMAL | Chip DMA Request Line (Chips) | 2,4 |
| DRA[8:0] | DRAM Address Bus (DRAM) | 2,3 |
| DRD[15:0] | DRAM Data Bus (DRAM) | 2,3,4,5 |
| DSR | Data Set Ready (RS232 Port) | 6 |
| DTACK | Data Transfer Acknowledge (68000) | 2,3,7 |
| DTR | Data Terminal Ready (RS232 Port) | 6 |
| E | Peripheral Enable Clock (68000) | 2,6,7 |
| EXTICK | Expansion Present / RTC Tick | 2,3 |
| FC[2:0] | Function Code (68000) | 2,7 |
| FIRE0/1 | Fire Button 0/1 (Joysticks) | 2,5,6 |
| HLT | Processor Halt (68000) | 2,7 |
| HSYNC | Horizontal Sync (Video) | 2,5,6 |
| INDEX | Index Pulse (Floppy) | 6,7 |
| INT[2,3,6] | Interrupt Request (Chips) | 2,4,6,7 |
| IORESET | I/O Reset | 6,7 |
| IPL[2:0] | Interrupt Priority Level (68000) | 2,4,7 |
| KBCLOCK | Keyboard Clock (Keyboard) | 6 |
| KBDATA | Keyboard Data (Keyboard) | 6 |
| KBRESET | Keyboard Reset (Keyboard) | 6 |
| LDS/UDS | Upper / Lower Data Strobes (68000) | 2,7 |
| LED | Power On LED / Audio Filter Disable | 4,6 |
| LEFT/RIGHT | Left Right Audio (Audio) | 4 |

| SIGNAL | DESCRIPTION (AREA) | PAGES |
|---|---|---|
| LPEN | Light Pen Trigger (Joysticks) | 2,6 |
| MTR | Motor On (Floppy) | 4,6 |
| MTR0 | Motor On - Drive 0 (Floppy) | 4,6,7 |
| M0V/M0H | Mouse 0 Quadrature V/H (Joysticks) | 5 |
| M1V/M1H | Mouse 1 Quadrature V/H (Joysticks) | 5 |
| OVL | Overlay ROM over RAM | 2,6 |
| OVR | Override System Decoding | 2,7 |
| PIXELSW | Genlock Pixel Switch (Video) | 5 |
| POT0X/0Y | Pot Lines 0 X/Y (Joysticks) | 4,5 |
| POT1X/1Y | Pot Lines 1 X/Y (Joysticks) | 4,5 |
| POUT | Paper Out (Parallel Port) | 6 |
| PPD[7:0] | Parallel Port Data (Parallel Port) | 6 |
| RAMEN | RAM Enable (Chips) | 2 |
| REGEN | Chip Register Enable (Chips) | 2 |
| RAS0/1 | Row Address Strobe (DRAM) | 2,3 |
| RDY | Drive Ready (Floppy) | 6,7 |
| RESET | General Reset | 6,7 |
| RGA[8:1] | Register Address Bus (Chips) | 2,4,5 |
| R/G/B | Red / Green / Blue (Video) | 5 |
| RI | Ring Indicate (RS232 Port) | 6 |
| ROMEN | ROM Enable (ROM) | 2,3 |
| RTS | Request to Send (RS232 Port) | 6 |
| RST | Processor Reset (68000) | 2,4,7 |
| RXD | Receive Data (RS232 Port) | 4,6 |
| RW | Processor Read/Write (68000) | 2,6,7 |
| SEL | Select (Parallel Port) | 6 |
| SEL[3:0] | Drive Select (Floppy) | 4,6,7 |
| SIDE | Side Select (Floppy) | 6,7 |
| STEP | Step In/Out Command (Floppy) | 6,7 |
| TRK0 | Track Zero Sense (Floppy) | 6,7 |
| TXD | Transmit Data (RS232 Port) | 4,6 |
| VMA | Valid Memory Address (68000) | 2,6,7 |
| VPA | Valid Peripheral Address (68000) | 2,7 |
| VSYNC | Vertical Sync (Video) | 2,5,6 |
| WE | Write Enable (DRAM) | 2,3 |
| WPROT | Write Protect Sense (Floppy) | 6,7 |
| XCLK | External Genlock Clock (Video) | 2,5 |
| XCLKEN | External Clock Enable (Video) | 2,5 |
| XRDY | External Data Ready | 2,5 |

# Key Components

| REF | CHIP | DESCRIPTION | PAGE |
|---|---|---|---|
| U1 | 68000 | 68000 Processor | 2 |
| U2 | 8370 | Fat Agnus - NTSC | 2 |
| | 8371 | Fat Agnus - PAL | alt |
| | 8372 | Agnus HR | alt |
| U3 | 8364 | Paula | 4 |
| U4 | 8362 | Denise | 5 |
| | 8373 | Denise HR | alt |
| U5 | 5719 | Gary | 2,4 |
| U6 | asst | ROM 128Kx16, 200 nS | 3 |
| U7-8 | 8520 | Amiga VIA, 1 MHz | 6 |
| U14 | LF347 | BiMOS Op-Amp | 4 |
| | TL084 | BiMOS Op-Amp | alt |
| U38 | 1488 | EIA Line Driver | 4 |
| U39 | 1489 | EIA Line Receiver | 4 |
| U42 | NE555 | Timer | 7 |
| U16-19 | asst | DRAM 1Mx1, 150 nS | 3 |
| U20-23 | asst | DRAM 1Mx1, 150 nS | 9 |
| X1 | OSC | TTL 28.63636 MHz NTSC | 2 |
| | OSC | TTL 28.37512 MHz PAL | alt |
| HY1 | asst | Video Hybrid | 5 |

ATTEMPT TO FORCE NODE NUMBERS VIA SEQUENCE

VCC +12V -12V +VID AUDIO EXP +5X +12X

A PAGE FOR SHARON AND VONNIE TO USE

| | | | |
|---|---|---|---|
| DRAWN BY: G. Robbins | DATE 04/27/89 | Commodore | |
| CHKD: | | Schematic A500 R6a/7<br>C/A500 Main Board<br>"Rock Lobster" | |
| ENGR: GRR | 09/09/88 | | |
| APPR: | | | |
| USED ON C/A500 | NEXT ASSY 312006 | SIZE C · 312007 | REV 1 |
| | | SCALE | SHEET 1 OF 8 |

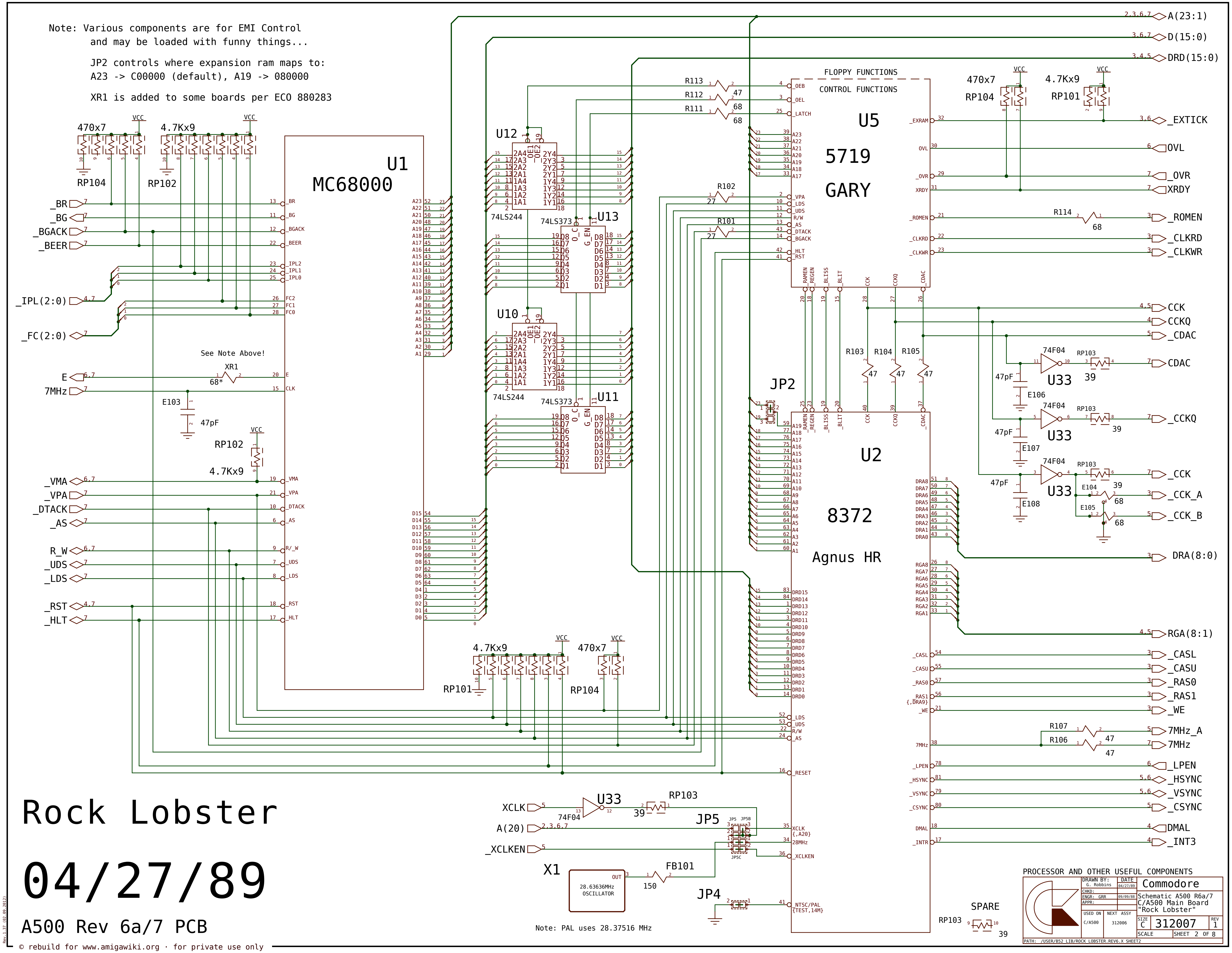
PATH: /USER/B52_LIB/ROCK_LOBSTER_REV6.X SHEET1

# A500 Rev 6a/7 PCB

Note: Various components are for EMI Control
and may be loaded with funny things...

JP2 controls where expansion ram maps to:
A23 -> C00000 (default), A19 -> 080000

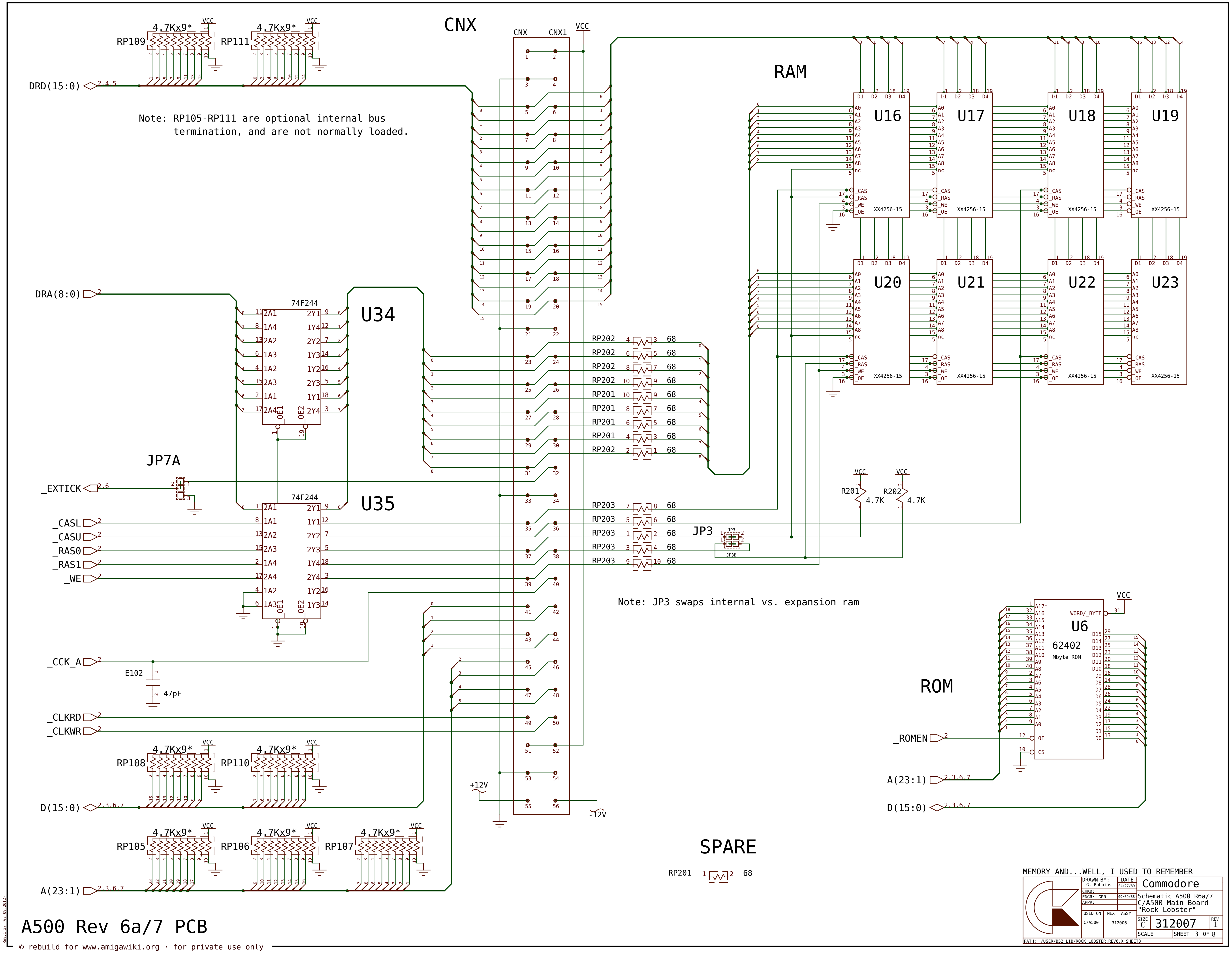
XR1 is added to some boards per ECO 880283



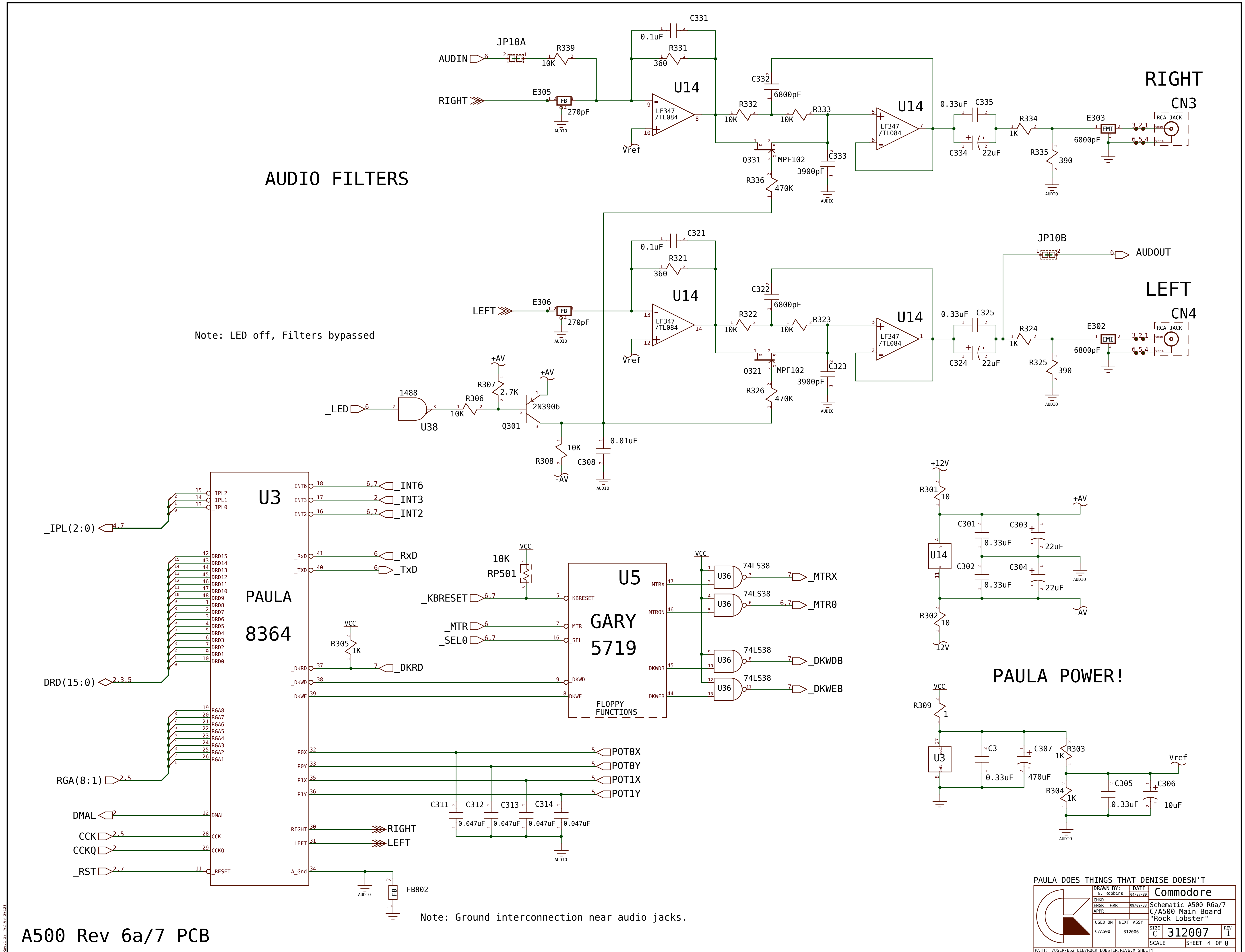

# Rock Lobster

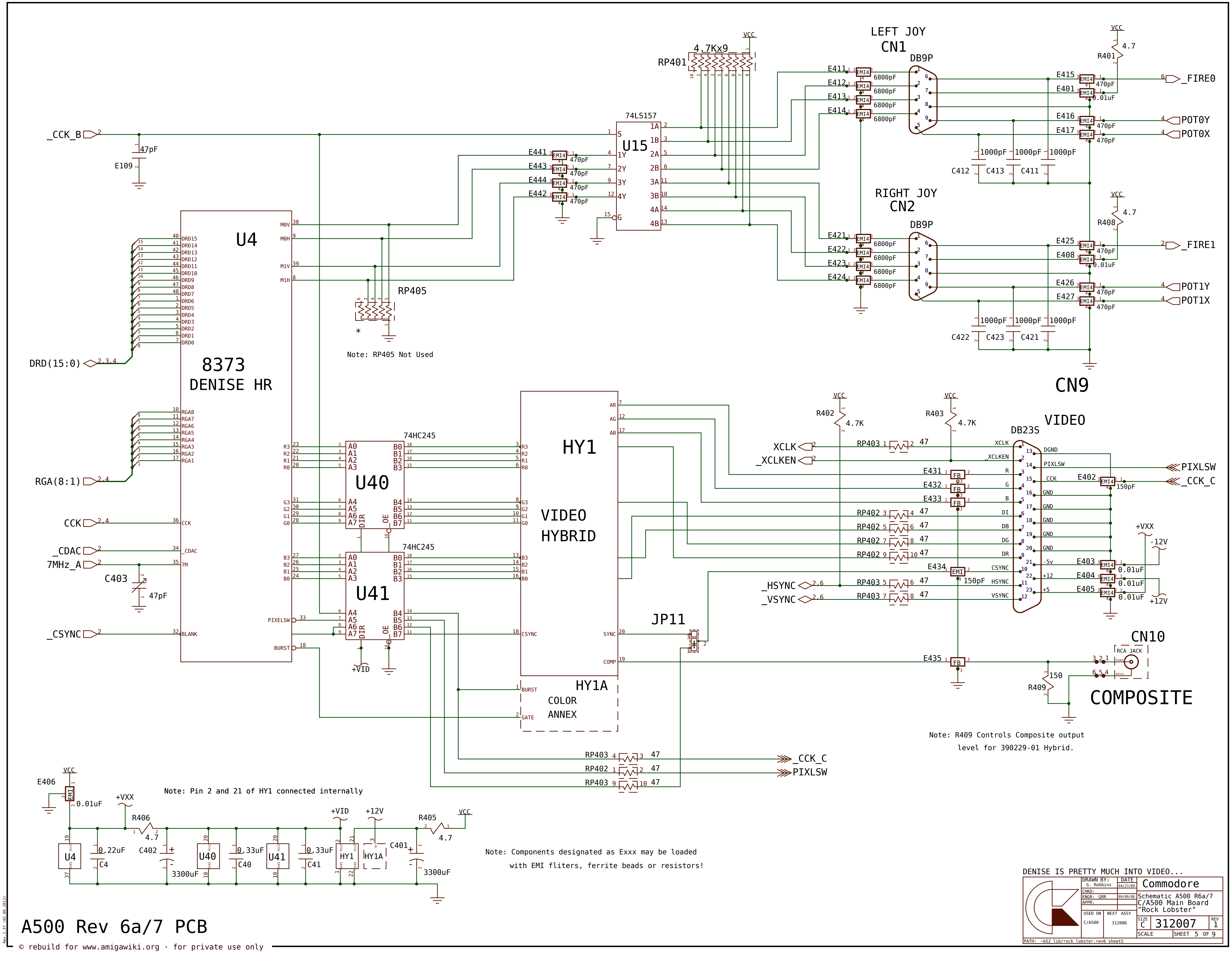
# 04/27/89

## A500 Rev 6a/7 PCB

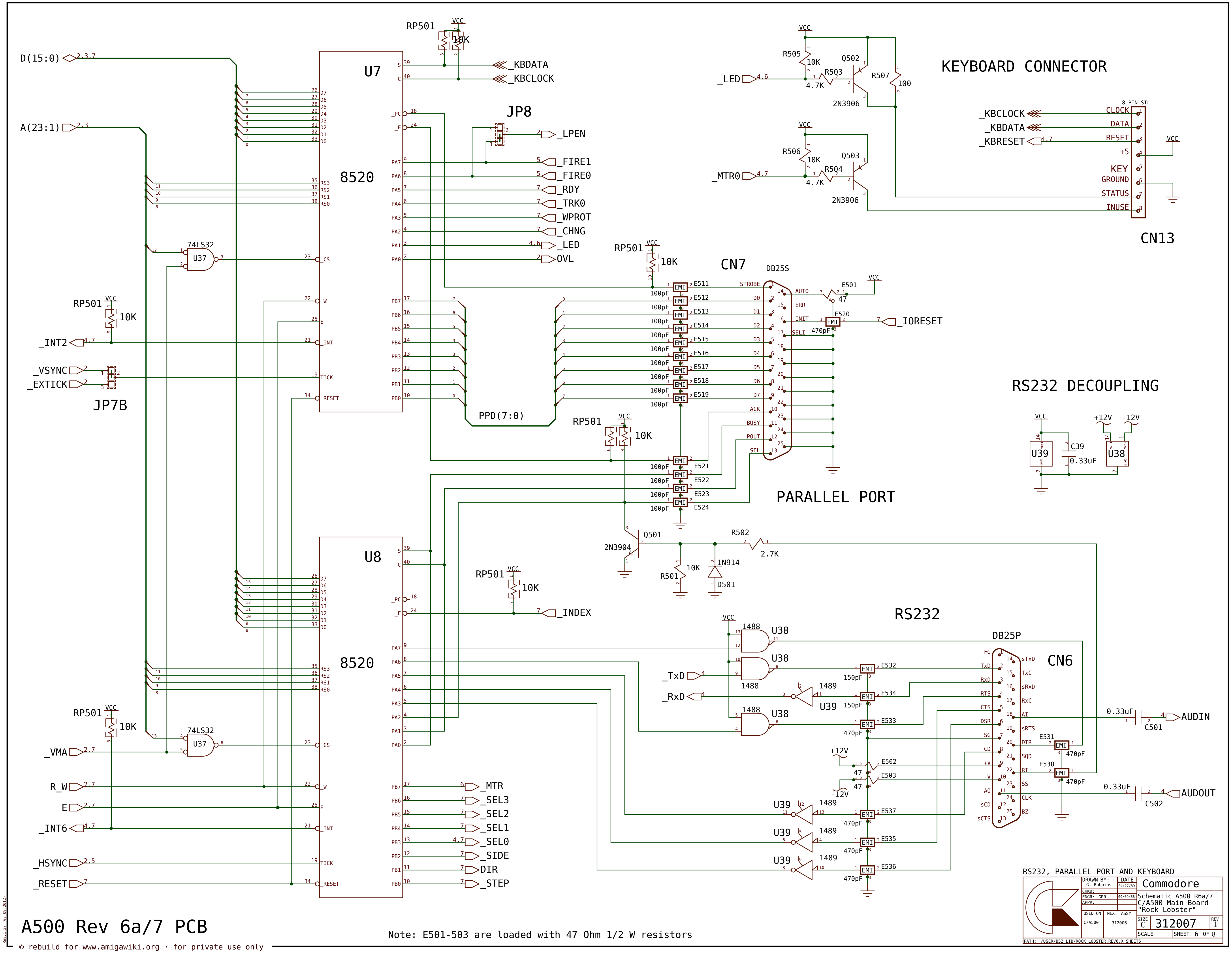


CNX
RAM
ROM
SPARE
Note: RP105-RP111 are optional internal bus termination, and are not normally loaded.
Note: JP3 swaps internal vs. expansion ram
RP109 4.7Kx9*
RP111 4.7Kx9*
RP108 4.7Kx9*
RP110 4.7Kx9*
RP105 4.7Kx9*
RP106 4.7Kx9*
RP107 4.7Kx9*
DRD(15:0)
DRA(8:0)
_EXTICK
_CASL
_CASU
_RAS0
_RAS1
_WE
_CCK_A
_CLKRD
_CLKWR
D(15:0)
A(23:1)
_ROMEN
JP7A
JP3
U34 74F244
U35 74F244
U16
U17
U18
U19
U20
U21
U22
U23
XX4256-15
U6 62402 Mbyte ROM
E102 47pF
R201 4.7K
R202 4.7K
RP201 68
RP202 68
RP203 68
VCC
+12V
-12V
MEMORY AND...WELL, I USED TO REMEMBER
Commodore
Schematic A500 R6a/7
C/A500 Main Board
"Rock Lobster"
DRAWN BY: G. Robbins
312007
SHEET 3 OF 8
A500 Rev 6a/7 PCB
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AUDIO FILTERS
Note: LED off, Filters bypassed
AUDIN
JP10A
R339 10K
RIGHT
E305
270pF
C331 0.1uF
R331 360
U14
LF347 /TL084
Vref
R332 10K
C332 6800pF
R333 10K
Q331 MPF102
R336 470K
C333 3900pF
0.33uF C335
C334 22uF
R334 1K
R335 390
E303 EMI
6800pF
RIGHT
CN3
RCA JACK
LEFT
E306
C321 0.1uF
R321 360
R322 10K
C322 6800pF
R323 10K
Q321 MPF102
R326 470K
C323 3900pF
0.33uF C325
C324 22uF
R324 1K
R325 390
E302 EMI
JP10B
AUDOUT
LEFT
CN4
_LED
1488
U38
R306 10K
+AV
R307 2.7K
2N3906
Q301
R308 10K
-AV
C308 0.01uF
AUDIO
U3
PAULA
8364
_IPL(2:0)
DRD(15:0)
RGA(8:1)
DMAL
CCK
CCKQ
_RST
_INT6
_INT3
_INT2
_RxD
_TxD
VCC
R305 1K
_DKRD
RIGHT
LEFT
FB802
POT0X
POT0Y
POT1X
POT1Y
C311 C312 C313 C314
0.047uF 0.047uF 0.047uF 0.047uF
10K
RP501
_KBRESET
_MTR
_SEL0
U5
GARY
5719
FLOPPY FUNCTIONS
74LS38
U36
_MTRX
_MTR0
_DKWDB
_DKWEB
+12V
R301 10
C301 0.33uF
C303 22uF
C302 0.33uF
C304 22uF
R302 10
-12V
PAULA POWER!
R309 1
C3 0.33uF
C307 470uF
R303 1K
R304 1K
C305 0.33uF
C306 10uF
Vref
Note: Ground interconnection near audio jacks.
PAULA DOES THINGS THAT DENISE DOESN'T
DRAWN BY: G. Robbins
DATE 04/27/88
ENGR: GRR
Commodore
Schematic A500 R6a/7
C/A500 Main Board
"Rock Lobster"
USED ON C/A500
NEXT ASSY 312006
SIZE C
312007
REV 1
SHEET 4 OF 8
PATH: /USER/852 LIB/ROCK LOBSTER.REV6.X SHEET4
A500 Rev 6a/7 PCB

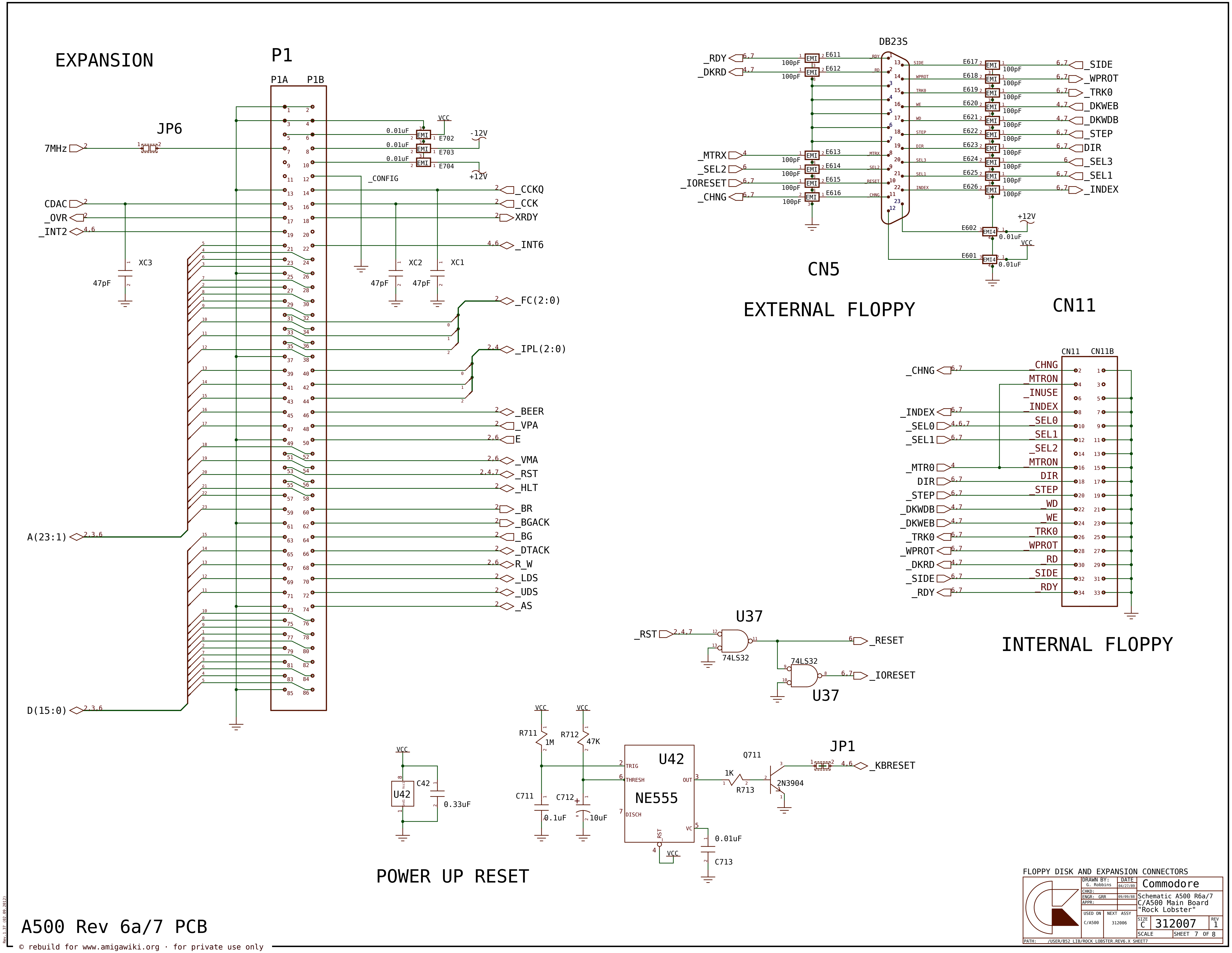


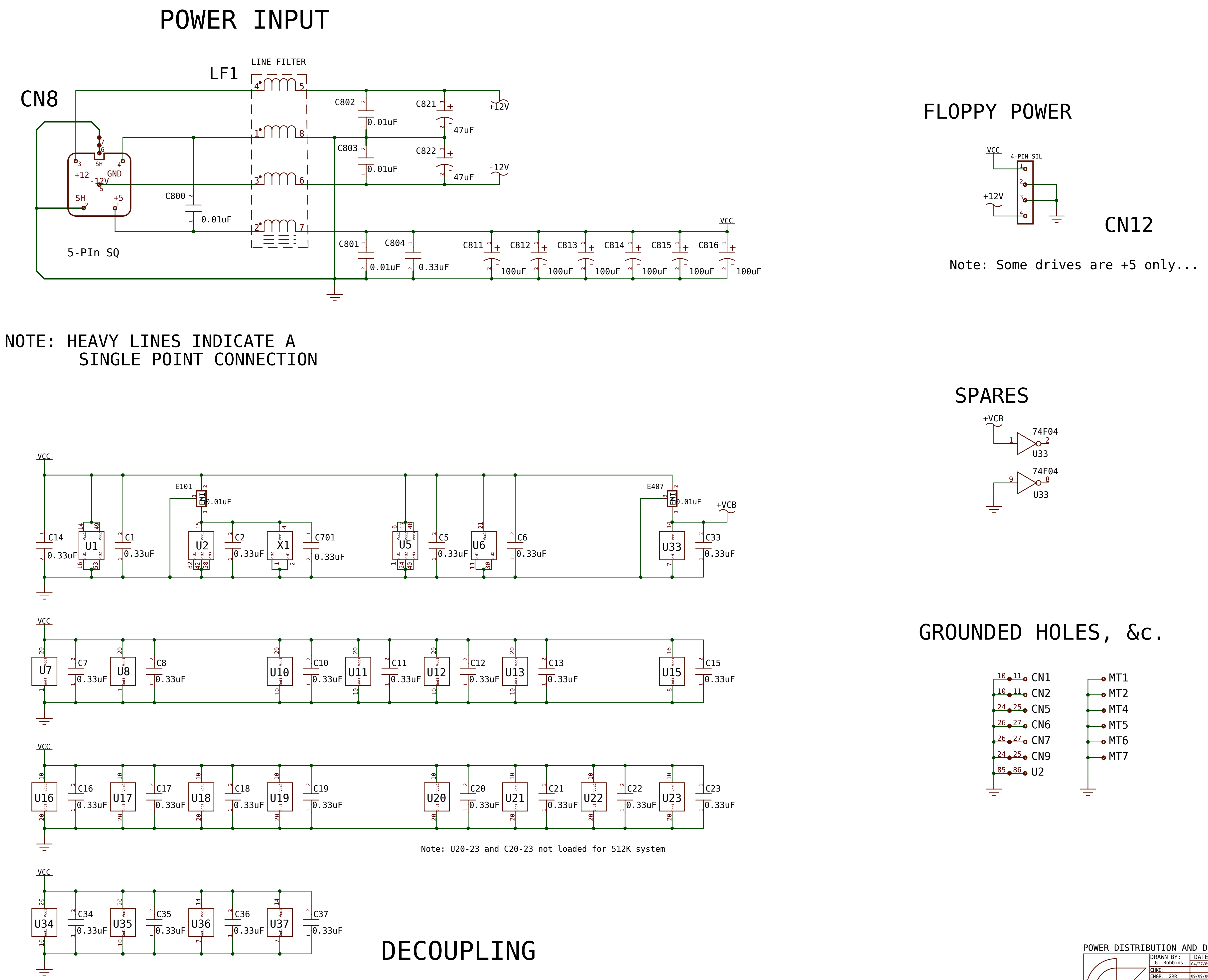

Rev.1.37 (02.09.2012)




# A500 Rev 6a/7 PCB

Note: E501-503 are loaded with 47 Ohm 1/2 W resistors


EXPANSION
P1
P1A P1B
JP6
7MHz
CDAC
_OVR
_INT2
XC3
47pF
A(23:1)
D(15:0)
0.01uF E702
0.01uF E703
0.01uF E704
VCC
-12V
+12V
_CONFIG
_CCKQ
_CCK
XRDY
_INT6
XC2
XC1
47pF
_FC(2:0)
_IPL(2:0)
_BEER
_VPA
E
_VMA
_RST
_HLT
_BR
_BGACK
_BG
_DTACK
R_W
_LDS
_UDS
_AS
DB23S
_RDY
_DKRD
_MTRX
_SEL2
_IORESET
_CHNG
100pF
E611
E612
E613
E614
E615
E616
E617
E618
E619
E620
E621
E622
E623
E624
E625
E626
E602
E601
0.01uF
_SIDE
_WPROT
_TRK0
_DKWEB
_DKWDB
_STEP
DIR
_SEL3
_SEL1
_INDEX
CN5
EXTERNAL FLOPPY
CN11
CN11 CN11B
_CHNG
_MTRON
_INUSE
_INDEX
_SEL0
_SEL1
_SEL2
_MTRON
_MTR0
DIR
_STEP
WD
_DKWDB
_WE
_DKWEB
_TRK0
_WPROT
RD
_DKRD
SIDE
_SIDE
RDY
_RDY
INTERNAL FLOPPY
U37
_RST
74LS32
_RESET
_IORESET
POWER UP RESET
U42
C42
0.33uF
R711 1M
R712 47K
C711 0.1uF
C712 10uF
NE555
TRIG
THRESH
DISCH
OUT
0.01uF
C713
Q711
1K
R713
2N3904
JP1
_KBRESET
FLOPPY DISK AND EXPANSION CONNECTORS
DRAWN BY: G. Robbins
DATE 04/27/88
CHKD:
ENGR: GRR 09/09/88
APPR:
Commodore
Schematic A500 R6a/7
C/A500 Main Board
"Rock Lobster"
USED ON C/A500
NEXT ASSY 312006
SIZE C
312007
REV 1
SCALE
SHEET 7 OF 8
PATH: /USER/B52 LIB/ROCK LOBSTER.REV6.X SHEET7
A500 Rev 6a/7 PCB
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POWER DISTRIBUTION AND DECOUPLING

| | | | |
|---|---|---|---|
| DRAWN BY: G. Robbins | DATE 04/27/89 | Commodore | |
| CHKD: | | Schematic A500 R6a/7 C/A500 Main Board "Rock Lobster" | |
| ENGR: GRR | 09/09/88 | | |
| APPR: | | | |
| USED ON C/A500 | NEXT ASSY 312006 | SIZE C 312007 | REV 1 |
| | | SCALE | SHEET 8 OF 8 |

PATH: /USER/B52_LIB/ROCK_LOBSTER.REV6.X SHEET6

# A500 Rev 6a/7 PCB

# Cake

04/27/89

A501 Rev 6c PCB

Notes: Some configurations of this RAM expansion require mods to rev 3 and 5 A500 boards and/or use of the Agnus HR 2MB bond-out.

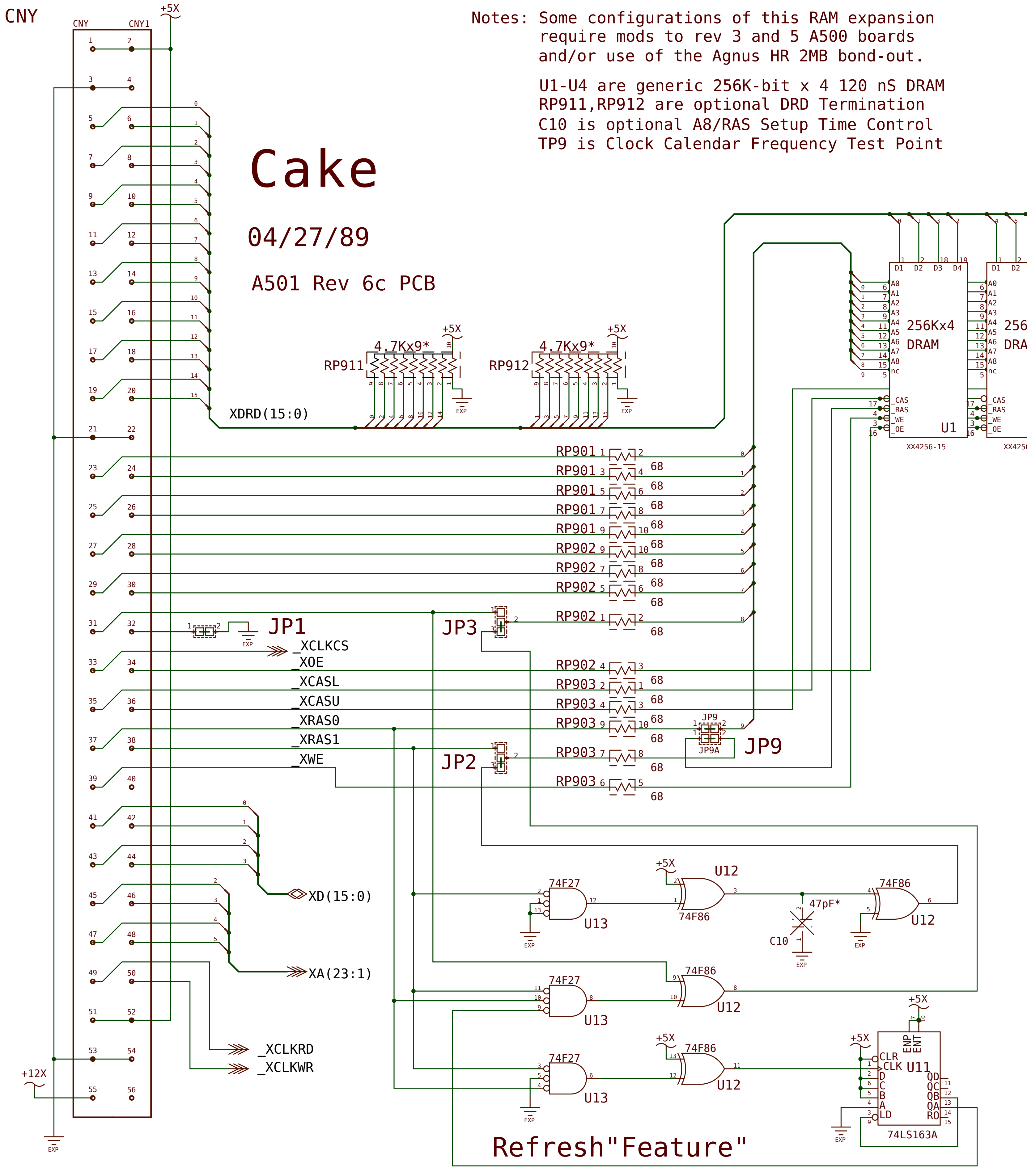
U1-U4 are generic 256K-bit x 4 120 nS DRAM
RP911,RP912 are optional DRD Termination
C10 is optional A8/RAS Setup Time Control
TP9 is Clock Calendar Frequency Test Point

## Revision History

| REV | DESCRIPTION | DATE | APRVL | MANAGER |
|---|---|---|---|---|
| 1 | Production | 03/19/89 | GRR | |
| | | | | |
| | | | | |
| | | | | |

## ECO History

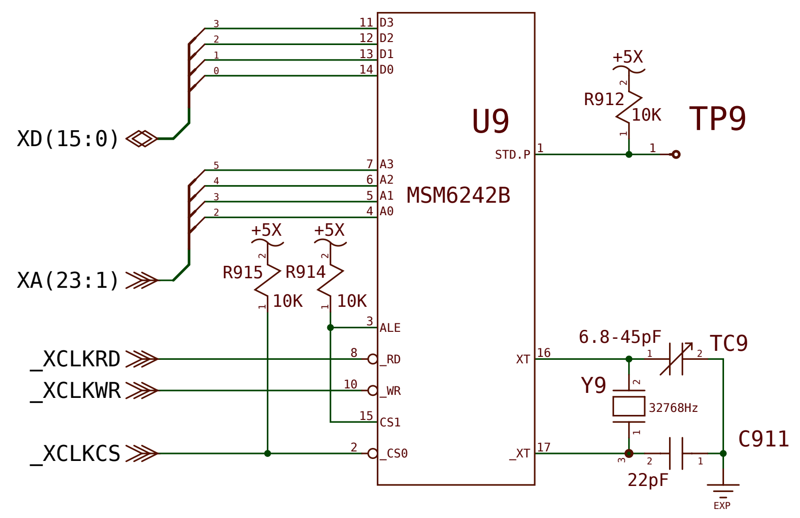
| ECO NUMBER | DESCRIPTION | DATE |
|---|---|---|
| | | |
| | | |
| | | |

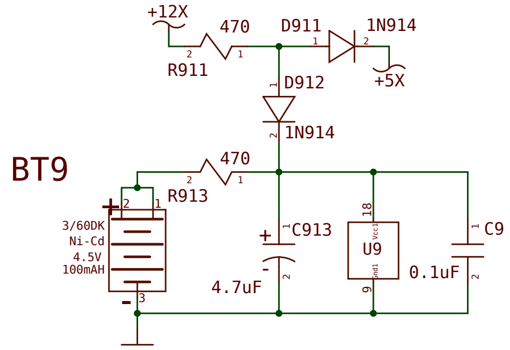



## Configuration Options

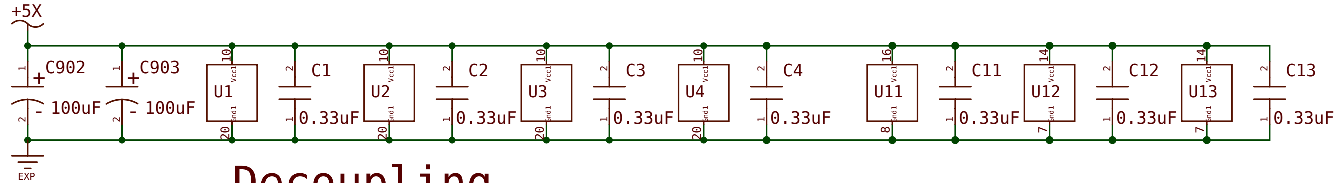
| | A | B |
|---|---|---|
| on-board | 512K | 2M |
| on A501 | 512K | - |
| U1-U4 | 256Kx4 | 1Mx4 |
| Agnus | Fat/HR | HR (2M) |
| JP1 | 1-2 | - |
| JP9 | 1-2,1-2 | 1-1,2-2 |

## Real Time Clock




## Real Time Power




## Decoupling...

512K/2M-BYTE RAM EXPANSION AND CLOCK

| DRAWN BY: G. Robbins | DATE 04/27/89 | Commodore |
|---|---|---|
| CHKD: | | |
| ENGR: GRR | 03/26/89 | Schematic, A501 R6c C/A500 512K Memory 1Mbit Flavor"Cake" |
| APPR: | | |
| USED ON C/A500 | NEXT ASSY 312987 | SIZE C 312988 REV 1 |
| | | SCALE SHEET 1 OF 1 |

PATH: /USER/852 LIB/CAKE.REV6.X SHEET1

Rev.1.37 (02.09.2012)